IN THE CLAIMS:

Please amend claims 1 and 24, and cancel claims 2 and 3 as follows:

1. (Currently amended) An integrated transceiver circuit, comprising:

a reception path ~~including~~ comprising:

a mixer unit ~~for demodulating~~ configured to demodulate a received signal[[,]] ;

~~and also including~~ an analog/digital converter unit connected downstream from the mixer unit;

a first voltage controlled oscillator;

a first frequency divider connected between the first voltage controlled oscillator and the mixer unit ~~for obtaining~~ , and configured to obtain a demodulation frequency for use by the mixer unit; and

a second frequency divider connected between the first voltage controlled oscillator and the analog/digital converter unit ~~for obtaining~~ , and configured to obtain a sampling frequency for use by the analog/digital converter unit; and

a transmission path comprising:

a modulator configured to modulate a signal to be transmitted;

a second voltage controlled oscillator;

a third frequency divider connected between the second voltage controlled oscillator and the modulator, and configured to obtain a modulation frequency for use by the modulator;

a digital/analog converter unit connected upstream of the modulator; and

a fourth frequency divider connected between the second voltage controlled oscillator and the digital/analog converter unit, and configured to obtain a sampling frequency for use by the digital/analog converter unit.

2. (Cancelled)

3. (Cancelled)

4. (Original) The integrated transceiver circuit of Claim 3, including a reference frequency input for receiving an external reference frequency, and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator.

5. (Original) The integrated transceiver circuit of Claim 4, including a second phase locked loop connected between the reference frequency input and the second voltage controlled oscillator.

6. (Original) The integrated transceiver circuit of Claim 5, wherein the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path.

7. (Original) The integrated transceiver circuit of Claim 6, wherein the reception path includes a digital/analog converter unit coupled to the output of the digital signal processing unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

8. (Original) The integrated transceiver circuit of Claim 4, wherein the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path.

9. (Original) The integrated transceiver circuit of Claim 8, wherein the reception path includes a digital/analog converter unit coupled to the output of the digital signal processing unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

10. (Original) The integrated transceiver circuit of Claim 3, wherein the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path.

11. (Original) The integrated transceiver circuit of Claim 10, wherein the reception path includes a digital/analog converter unit coupled to the output of the digital signal processing unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

12. (Original) The integrated transceiver circuit of Claim 3, including a reference frequency input for receiving an external reference frequency, and a phase locked loop connected between the reference frequency input and the second voltage controlled oscillator.

13. (Original) The integrated transceiver circuit of Claim 3, wherein the transmission path includes a low-pass filter unit connected between the digital/analog converter unit and the modulator.

14. (Original) The integrated transceiver circuit of Claim 2, wherein the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms an digital output of the reception path.

15. (Original) The integrated transceiver circuit of Claim 14, wherein the reception path includes a digital/analog converter unit coupled to the output of the digital signal processing unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

16. (Original) The integrated transceiver circuit of Claim 2, including a reference frequency input for receiving an external reference frequency, and a phase locked loop connected between the reference frequency input and the second voltage controlled oscillator.

17. (Original) The integrated transceiver circuit of Claim 16, including a further phase locked loop connected between the reference frequency input and the first voltage controlled oscillator.

18. (Original) The integrated transceiver circuit of Claim 2, including a reference frequency input for receiving an external reference frequency, and a phase locked loop connected between the reference frequency input and the first voltage controlled oscillator.

19. (Original) The integrated transceiver circuit of Claim 2, wherein the modulator is an IQ modulator.

20. (Original) The integrated transceiver circuit of Claim 1, wherein the analog/digital converter unit includes first and second analog/digital converters having respective sampling control inputs which are connected to an output of the second frequency divider.

21. (Original) The integrated transceiver circuit of Claim 1, wherein the reception path includes a low-pass filter unit connected between the mixer unit and the analog/digital converter unit.

22. (Original) The integrated transceiver circuit of Claim 1, wherein the mixer unit is an IQ mixer.

23. (Original) The integrated transceiver circuit of Claim 1, wherein the first and second frequency dividers are integer dividers.

24. (Currently Amended) A method for processing a signal, comprising:

obtaining a demodulation frequency for use by a mixer unit in a reception path of an integrated transceiver circuit with a first frequency divider connected between a first voltage controlled oscillator and the mixer unit;

demodulating a received signal with the mixer unit and the obtained demodulation frequency;

obtaining a sampling frequency for use by an analog to digital converter unit with a second frequency divider connected between the first voltage controlled oscillator and the analog to digital converter unit; ~~and~~

performing a digitizing operation on the demodulated received signal with the analog to digital converter and the obtained sampling frequency;

obtaining a modulation frequency for use by a modulator in a transmission path of the integrated transceiver circuit with a third frequency divider connected between a second voltage controlled oscillator and the modulator;

modulating a signal to be transmitted with the modulator and the obtained modulation frequency;

obtaining a sampling frequency for use by a digital to analog converter unit with a fourth frequency divider connected between the second voltage controlled oscillator and the digital to analog converter unit; and

performing a de-digitizing operation on the modulated received signal with the digital to analog converter and the obtained sampling frequency.